Integrated Green-niX+ Research Unit

Overview

Semiconductor integrated circuits have advanced speed and power consumption reduction based on device scaling. In our unit, we are conducting research on 3D integration of FETs, thermoelectric elements, and devices using 2D materials, aiming for further miniaturization and higher performance. In particular, FETs using transition metal dichalcogenides, which are atomic layered materials, are attracting attention at academic societies as materials that can maintain high performance even if the generation is 2 nm or less.
In addition to these research activities, we are operating three consortiums, the Integrated Green-niX Research and Human Resource Development Center, Industry-University Consortium for the Integrated Systems and Materials, and the EISESiV Consortium, under a Keep-neutral scheme that maximizes mutual collaboration and cooperation.

Research Unit Leader **Hitoshi Wakabayashi**

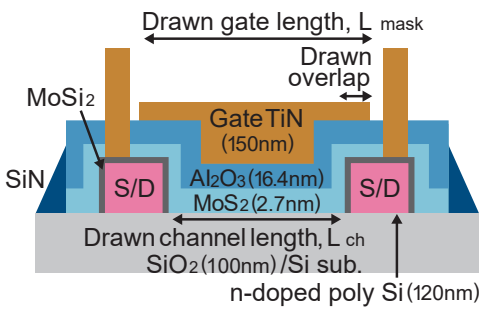
Profile

2023 Professor, Institute of Innovative Research, Tokyo Institute of Technology
2016 Professor, Engineering,Tokyo Institute of Technology.
2013 Professor, Interdisciplinary Granduate School of Science and Engineering, Tokyo Institute of Technology.
2006 SONY Corporation
2000 Massachusetts Institute of Technology, Microsystems Technology Laboratories, Visiting Scientist
1993 NEC Corporation

Research Goals

Semiconductor integrated circuits have made dramatic progress for more than half a century, based on the scaling of MOSFETs. On the other hand, in recent years, social issues such as climate change have surfaced, and in the future research and development that considers not only convenience and economic efficiency but also social rationality is desired.
In addition to improving performance, this unit promotes research activities on semiconductor integrated circuits with a focus on greening manufacturing and reducing power consumption of integrated circuits. We are looking to implement.
In the research of two-dimensional semiconductor devices, which is a particular focus, we are proposing new device structures while selecting manufacturing methods such as sputtering and ALD on the assumption that they will be mass-produced by companies in the future, which is our strengths. By implementing this device as an integrated circuit in the generation of 2 nm or less, we aim to become a green semiconductor that achieves significant reductions in power consumption while supporting complex AI calculations.

Cross sectional schematic illustration of FET with MoS_2 channel, which is a typical 2-dimensional material.



source:
K. Matsuura, H. Wakabayashi et.al.,
"Normally-off sputtered-MoS_2 nMISFETs with TiN top-gate electrode all defined by optical lithography for chip level integration."
Japanese Journal of Applied Physics, 59, 2020.