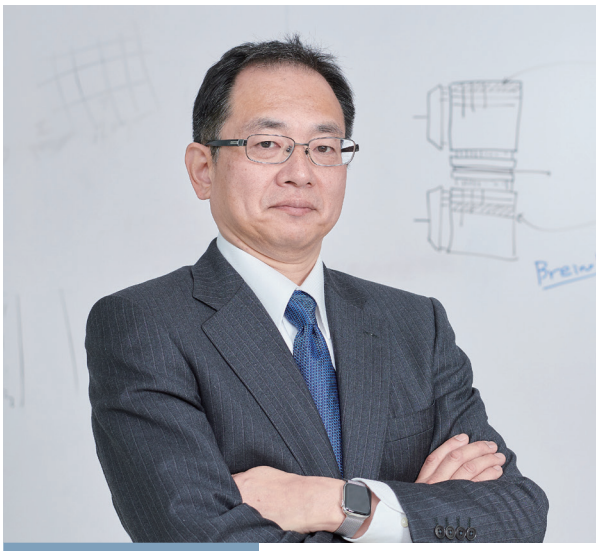
Tokyo Tech
Research Units

AI Computing Unit

Overview

In recent years, great strides in artificial intelligence (AI) have been made, with deep neural networks (DNN) at the center. However, AI computing is not limited to DNN but covers a broad range of machine learning fields, and also extends into data mining and big data processing. To traverse these realms exhaustively and efficiently utilize vastly increasing data, new hardware, rather than an extension of existing hardware, must be developed. The aim of this research unit is to establish the research and development infrastructure for hardware that will make the next generation of AI computing possible: technology that is markedly higher in energy and cost efficiency than what is currently available and also superior in autonomy and safety. We also aim to create a place for more people to participate in this field and flourish in industry-academia collaboration.



Research Unit Leader **Masato Motomura**

Profile

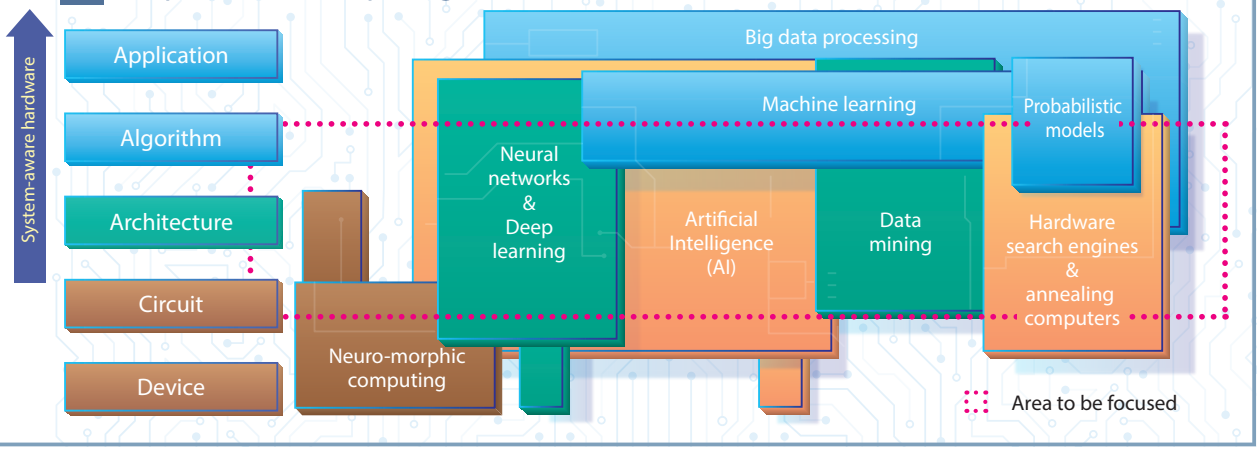
2019 Professor, Institute of Innovative Research, Tokyo Institute of Technology
2011 Professor, Course of Electronics for Informatics, Graduate School of Information Science and Technology, Hokkaido University
2009 NEC System IP Core Research Laboratories
2004 NEC Electronics Corporation
2001 NEC Electron Devices
1996 Doctor of Engineering, Kyoto University
1992 NEC Silicon Systems Research Laboratories
1991 Visiting Researcher, Massachusetts Institute of Technology
1987 NEC Microelectronics Research Laboratories
1987 Master of Science, Kyoto University

Research goals

I have worked for many years in reconfigurable hardware, a type of hardware which allows changes to be made to its circuit configuration according to what is being processed. What is special about this architecture is that, since it allows computing to always be performed using the optimum hardware configuration, processing speed is faster than conventionally possible, as well as highly energy efficient. Furthermore, since it can make use of large-scale data processing structures in parallel processing, it is highly compatible with AI computing. Since fiscal year 2018, with this architecture as a basis, we have been advancing AI computing through projects under the Grant-in-Aid for Scientific Research (S), New Energy and Industrial Technology Development Organization (NEDO), and Japan Science and Technology Agency (JST). Though the specific field of AI computing investigated in each project differs, this research unit will provide the R&D infrastructure enveloping all of these fields. In the future, I hope this unit will grow to become Japan's central facility for AI computing research.

An architecture platform that will drive AI computing

Map of the AI computing field



Working to develop innovative hardware and bring forth the next generation of AI computing

Q Why was this research unit established?

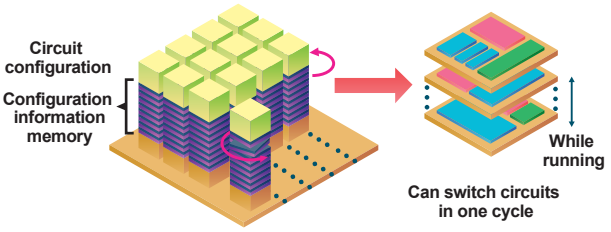
Computing on existing computers is done using a "procedural" approach, where commands are executed in serial. However, a "structural" approach, where data can be used as is and processed in parallel, is more suitable for AI. Another factor is that progress in microfabrication technology for semiconductors is reaching its end. With such issues, reconfigurable hardware is gaining attention as the computing technology that will allow for next-generation structural information processing. But for this to become a reality, AI algorithm and system-aware hardware research need to be coordinated and pursued with agility. As we spread the importance of this goal throughout the world, I also hope to cultivate new talent to carry on in this field in the future.

Q What are the strengths of this research unit?

Much research is being done worldwide in AI computing architecture, but most focuses on how to use existing computers in parallel. Meanwhile, there are many original technologies in the field of reconfigurable hardware that were developed in Japan. Even when viewed globally, we are ahead in technology and in accomplishments. For this reason, by focusing on reconfigurable hardware technology and collaborating closely with various research institutions and industries in AI, I believe we can become a dominant force in this global, highly competitive field of AI computing.

Reconfigurable hardware

Multiplex configuration information architecture and circuit



Unlike traditional logic circuits with fixed functions, reconfigurable hardware allows for changes in circuit configuration according to application needs. The AI Computing Unit is developing hardware offering even greater flexibility and software-friendliness, capable of dynamically changing configuration, even while running.

Q What is the path to achieving the unit's goals?

First, within the next several years, in each field of AI computing we aim to prototype reconfigurable hardware that is capable of high-speed processing and two orders of magnitude more energy efficient than existing designs. The target is an AI computing engine for built-in systems in vehicles, robots, IoT devices, and other applications that will utilize edge computing. It is important to foresee where AI algorithms are headed and have a meta-level architecture with the flexibility to adopt new ideas. We will also work on forming the basis for coordinating between software and hardware.

Contact us

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AI Computing Unit

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