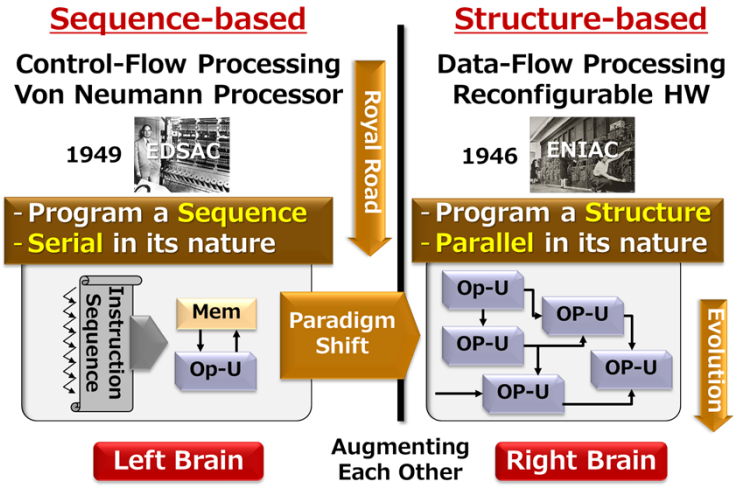
Motomura Laboratory

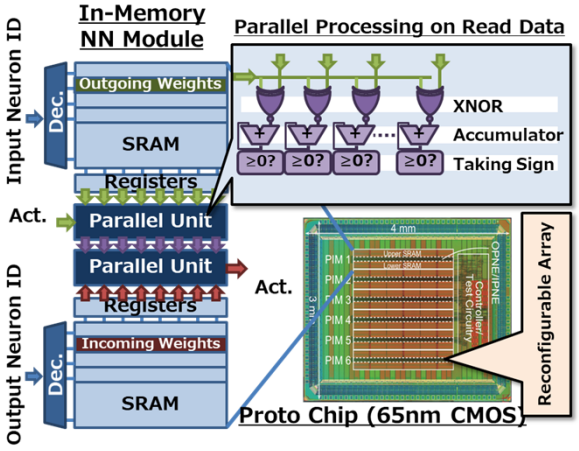
Establishing next-gen. AI computing architectures

AI Computing Research Unit
also Laboratory for Fuure Interdisciplinary Research of Science and Technology

- Deep learning and deep neural network accelerators
- Parallel annealing machines for optimization problems
- Softened hardware: Reconfigurable systems
- Structure-oriented computing architectures

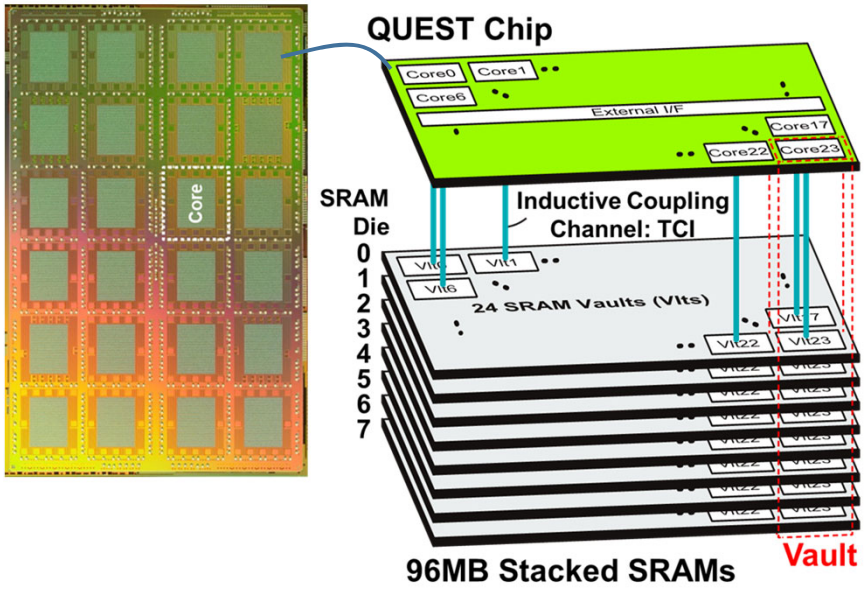
As the advent of deep neural network (DNN) technologies, AI computing applications are rapidly spreading. In contrast to traditional procedure-oriented ones, structure-oriented workloads become critically important in this new domain. Establishing computing architectures to accommodate such a fundamental change will enhance performance and energy efficiency of computing systems drastically.





Benchmark Results (Digit Recognition)

	BRein Memory	FPGA	GPU	CPU
Energy Efficiency Ratio	26K	33	9	1



Binary, Reconfigurable, in Memory DNN Accelerator LSI(BRein Memory)

Symposium on VLSI Circuits (Jun, '17). World-first binary DNN chip. Achieved x3K energy efficiency in comparison to CPU.

Log-Quantized DNN Engine with 3D Stacking Technology (QUEST)

ISSCC (Feb. '18). World first log-quantized and 3D-integrated DNN chip. Won Silkroad Award at the ISSCC.