# Tsutsui Lab

# Fabrication process and analyses for high performance semiconductor devices

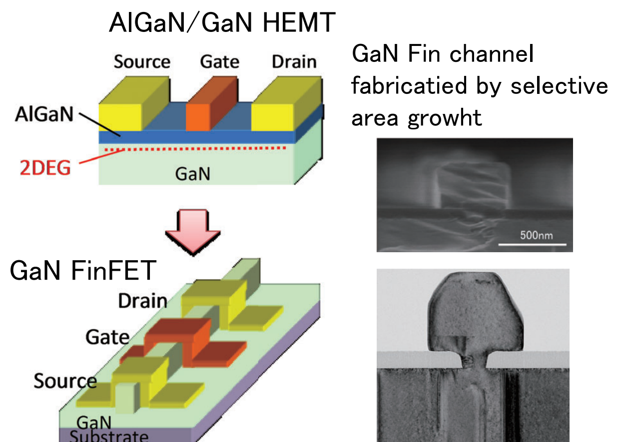
FIRST Applied Electronics Research Core

http://www.tsutsui.ep.titech.ac.jp/

- Scaling of Si power devices (IGBTs)
- New structures and processes for GaN power devices
- Analyses of dopants in semiconductors using photoelectron holography method

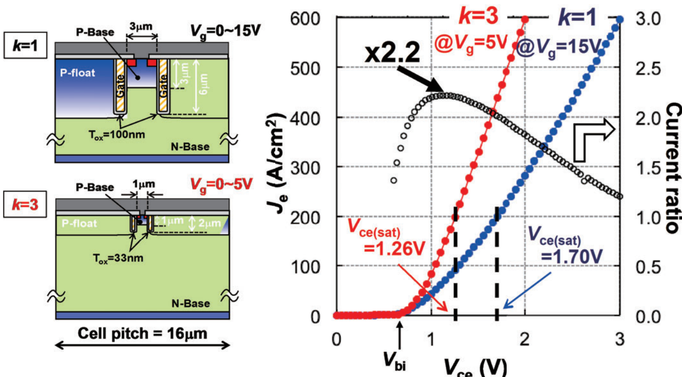
Device structures and fabrication process techniques for Si and GaN electron devices, especially focused to power devices, are investigated to realize next generation high performance devices.

Three dimensional atomic arrangements of dopants in semiconductors are analyzed using the photoelectron holography method. It will contribute developments of doping technologies to semiconductors, which is a significant technology for various semiconductor devices.



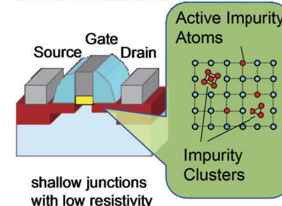

**GaN-FinFETs (3D channel strucutre) using selective area growth technique**

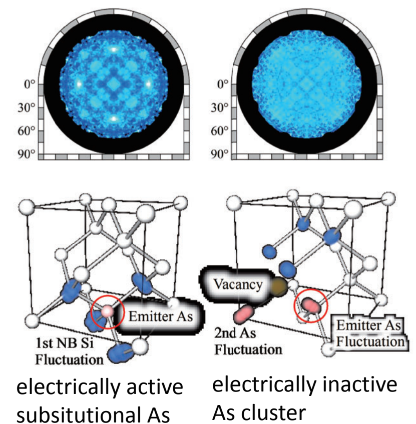
– Channels composed of GaN with good crystarinity.
– Hier performances beyond the conventional HEMTs.




**Scaling of Si power devices (IGBT)**

- Reducing internal power loss of IGBTs (insulated gate bipolar transistors) by scaling (miniaturization) of gate structures enhancing carrier accumulation.
- Theoretical expectation was experimentally revealed.




**3D atomic arrangements of As doped in Si revealed by photoelectron holography method**

- Not all doped As in Si are electrically active. Some As atoms are electrically inactive so as to degrade device performance.
- Atomic arrangements of the As atoms in the various states were revealed by the photoelectron holography method, correlating with electrically active/inactive.