SUGAHARA LAB.

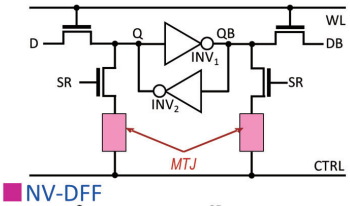
Integrated Electronics for Smart Mobile Devices and Internet-of-Humans

■ CMOS Integrated circuits ■ Micro thermoelectric generators ■ New functional transistors

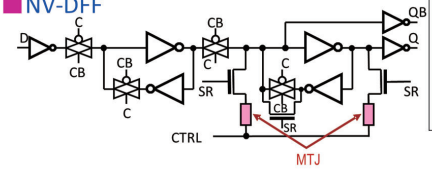
FIRST, Imaging Science and Engineering Research Center

●Power Gating Architecture Using Nonvolatile Retention

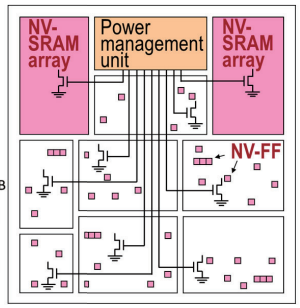
■NV-SRAM



■NV-DFF



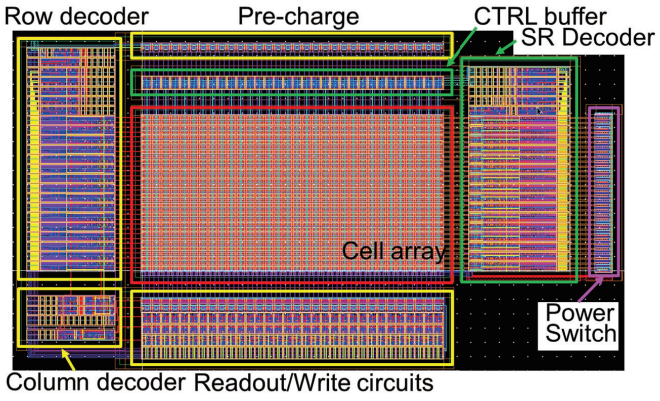
■Nonvolatile power gating:NVPG



•Nonvolatile bistable retention/memory circuits based on NVM/CMOS hybrid technology

•NVPG architecture using nonvolatile bistable retention/memory circuits

■Fabrication of NV-SRAM

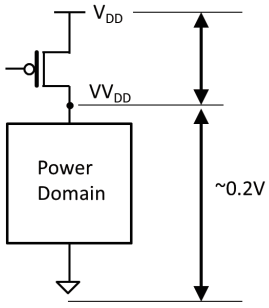


•Demonstration of NV-SRAM using 65nm CMOS process

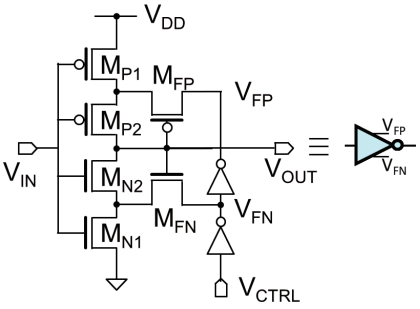
•NVPG is highly effective at reducing standby power

●NVPG Using Virtually Nonvolatile Retention Circuits

■ VV_{DD} retention concept



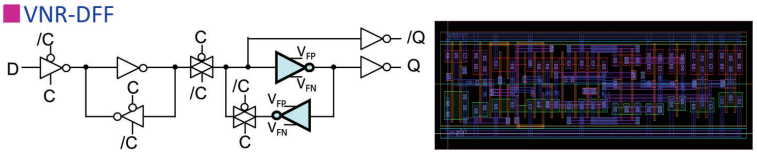
■Dual mode inverter



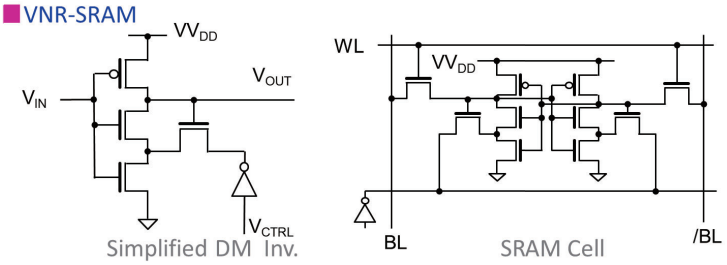
•Virtually nonvolatile retention (VNR) using virtual supply voltage (VV_{DD})

•Dual mode inverter:
-Boosted inverter (BI) mode: Fast operation at $VV_{DD} = V_{DD}$
-Schmitt trigger (ST) mode: Ultralow voltage retention at VV_{DD} =~0.2V

■VNR-DFF



■VNR-SRAM

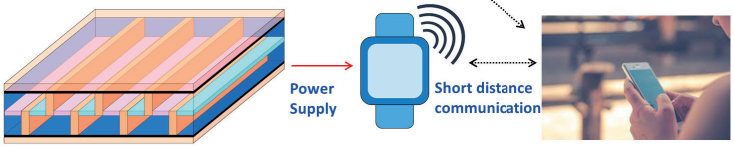


•VNR-DFF and VNR-SRAM configured with DM inverters

•NVPG can also be achieved using VNR retention/memory circuits

●Micro Thermoelectric Generators for WDs

■ Internet-of-Humans (IoH)



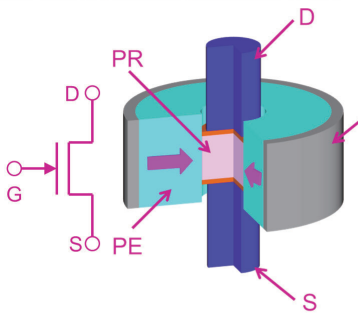
■Thin-film micro thermoelectric generator

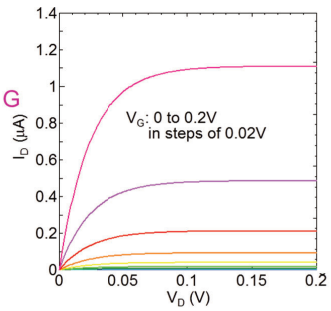
■ Wearable Device

■ Smart phoine /Wireless LAN

●Ultralow-voltage High-Speed Transistors

■Piezoelectronic transistor (PET)





•Piezoresistive channel + Piezoelectric gate
→Switching based on pressure-induced metal-insulator transition

•High current drivability at ultralow voltage

•Low leakage

•CMOS compatible